(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
28 November 2002 (28.11.2002)

PCT

(10) International Publication Number
WO 02/095914 A2

(51) International Patent Classification[7]: H02M

(21) International Application Number: PCT/US02/22513

(22) International Filing Date: 6 February 2002 (06.02.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/266,789 6 February 2001 (06.02.2001) US

(71) Applicant *(for all designated States except US)*: CROWN AUDIO, INC. [US/US]; 1718 West Mishawaka Road, P.O. Box 1000, Elkhart, IN 46515 (US).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: STANLEY, Gerald, R. [US/US]; 59766 Beech Road, Osceola, IN 46561 (US).

(74) Agent: GROEN, Eric, J.; Baker & Daniels, 205 West Jefferson Boulevard, Suite 250, South Bend, IN 46601 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

WO 02/095914 A2

(54) Title: HALF-BRIDGE GATE DRIVER CIRCUIT

(57) Abstract: A half-bridge gate driver cicuit including two separate floating high-side driver cicuits (8 and 8') for operating a switch cicuit having a high-side switch (7) and a low-side swich (9). Each of the driver cicuits (8 and 8') include input control logic wich is referenced to a supply signal with a potential that becomes negative relative to the negative common terminal (12) of the switches, thereby enchancing the operation of the switch cicuit. The circuit may further include signal translation stages (70) for translation control signals to the control logic of the driver cicuits (8 and 8'). The signal translation stages (70) include a plurality of cascoded parasitic transistor (71) which provide a neutralizing capacitance to minimize noise.

HALF-BRIDGE GATE DRIVER CIRCUIT

The present invention relates to switch-mode, half-bridge power circuits using gated devices, and, more particularly, to opposed current, power converter circuits driven by integrated circuit gate drivers with internal floating gate driver sections.

Modern half-bridge power circuits are frequently driven by integrated circuit (IC) gate drivers with internal floating gate driver sections driving the more positive voltage high-side of the half-bridge. The high-side and low-side input control signals are supplied common to the most negative portion of the IC. When IC gate drivers are used in high-voltage, hard-switching, half-bridge power converters, a problem can arise at the turn-off of the positive voltage high-side switch of the half-bridge. In this situation, the instantaneous voltage on the source lead of the high-side switch can momentarily go negative relative to the negative substrate of the IC. The principal reason for the voltage spike is that in a hard-switching converter, the free-wheeling diode cannot become fully conductive instantaneously. The free-wheeling diode's forward voltage can thus become rather large during this time delay compared to what would be expected in the DC case. In the transient case, the diode appears as a very high resistance device and may have 20 volts forward-biased across it. The 20 volt forward bias may last for approximately 10 to 20 nanoseconds until the diode becomes fully injected. The result is that the gate drive voltage goes negative with respect to the negative substrate of the IC with 20 volts plus any additional voltage due to inductance. As a result, the IC may cause a malfunction of the driver logic resulting in failure of the power stage by simultaneous conduction of the power switches or direct destruction of the gate driver IC. At a minimum, noise will be introduced into the system.

Methods have been developed to attempt to correct this problem. One method attempts to reduce the added voltage generated by the intrinsic inductance in the circuit, thereby decreasing the negative voltage spike imposed on the IC at the turn-off of the positive switch. This method has a serious drawback in the field of the present invention. Even if a designer were to compensate for all inductances in the construction of the circuit, the transient forward voltage across the free-wheeling diode would still be present in the circuit.

Attempting to compensate for the intrinsic inductance in the circuit fails to provide a successful solution in fast-switching, high-frequency applications since the forward

voltage produced by the free-wheeling diode will still cause simultaneous conduction of the power switches or direct destruction of the gate driver IC.

The known prior art subject to Figure 1, discloses a gate driver circuit for a half-bridge derived switching power converter having high voltage and hard switching characteristics. The gate driver circuit includes both a positive switch and a negative switch. A high side driver circuit operates the positive switch, while a low side driver circuit operates the negative switch. In addition, both switches are coupled to the same negative potential

Another problem of conventional designs is that they have a slower high-side gate driver due to the increased number of cascaded stages in the high-side gate driver as compared to the low-side gate driver. Some designs attempt to match the propagation delay between the high-side and low-side outputs by adding delays in the low side path. A typical method of adding such delays is to cascade an even number of inverters. Despite this effort, the result of the increased number of cascaded stages is imprecise timing in the circuit resulting in common-mode currents or shoot-through. The imprecise timing becomes particularly problematic when attempting to maintain timing over both time and temperature variations. Tolerances of the power switches, gate drive resistors, temperature thresholds, imperfections of the IC, and other parameters must be accounted for. When the tolerances are loose, increased distortion occurs in certain applications, for example, pulse-width modulated (PWM) audio amplifiers.

The present invention provides a circuit for minimizing the effects on gate driver ICs of high-voltage, hard-switching such as when driving opposed current power converters and other similar applications. The present invention overcomes the shortcomings of the prior art by utilizing two separate high-side gate drivers to drive an opposed current power converter, as opposed to the conventional, single high-side gate driver together with a low-side gate driver.

The invention, in one form thereof, comprises a switch-mode opposed current power converter with two separate floating high-side gate drivers. The removal of the low-side driver from the circuit permits the negative substrate potential of the IC to be as negative as necessary to protect the IC. The result is maximum isolation between the control signals for desired applications. The isolation between the control signals reduces the harmful effect of noise generated by the transition of one switch on the modulation

process of another switch. The isolation benefits gained by the present invention allow for a single IC to incorporate multiple high-side gate drivers. The present invention has various applications including, for example, audio amplifiers and three-phase motors which require an IC with six high-side gate driver stages.

The high-side design construction operates both the high-side and low-side switches with input control logic referenced to a supply with a negative substrate potential which, in operation, becomes negative with respect to the negative common terminal of both power switches. In effect, the negative substrate potential will be as negative as the most negative spike of forward voltage produced by the free-wheeling diode at the turn-off of the positive switch, thereby preventing a malfunction of the driver logic and destruction of the gate driver IC.

The input control logic reference supply voltage can be produced from a variety of sources. A battery could provide the necessary voltage, although this adds complexity and cost to the system. In one exemplary embodiment, the reference supply voltage is acquired by manipulating the forward recovery voltage of the free-wheeling diode to obtain the necessary voltage required to protect the IC. In another embodiment, the input control logic supply voltage is acquired by the use of an AC power supply already present in the circuit. The above-described embodiments provide the necessary voltage to the input control logic without increasing cost or introducing the added complexity associated with an extra power supply.

In one embodiment of the present invention, a signal translation stage may be included to provide a front-end scheme of translating the input signals to the control logic of the gate drivers. The signal translation stage can be used to correct for noise issues associated with the input signals to the control logic of the gate drivers. The compensation of the signal translation stage is equally useful in correcting noise issues whether they originated on the negative supply voltage ($-V_{cc}$) or were a product of the derived reference supply voltage ($-V_{cx}$) as further derived below. A signal translation stage includes three or more cascaded transistors with the associated bypass capacitors and resistors to more easily dissipate the noise incident on the control logic from the input signals. Also included in the signal translation stage are parasitic transistors which form the appropriate nonlinear capacitance to track voltages in the cascaded chain, and to properly cancel the effects of noises on the $-V_{cx}$ supply. The transistors utilized in the construction of the

signal translation stage include, but are not limited to, those shown in the drawings. One skilled in the art could readily adapt other types of transistors to the present application. An exemplary embodiment of the signal translation stage is a unique type of high-side gate driver IC which translates the signal from ground to the negative potential of the $-V_{cx}$ supply.

An advantage of the present invention is that it permits a negative voltage spike on the source lead of the high-side power switch without risking the dysfunction of the converter or other damage to the IC.

Another advantage of the present invention is that the symmetric design allows the propagation delays of the IC to be more uniform for both the high-side and low-side power switches.

Still another advantage of the present invention is the minimization of the quiescent output ripple for an interleaved converter.

A still further advantage of the present invention is a more complete isolation of the input from the output of the driver, thereby reducing noise incident on the input.

Yet another advantage of the present invention is the maximization of the drain source voltage on the internal gate driver translating field effect transistors, thereby reducing the propagation delay of the high-side driver.

The above-mentioned and other features and advantages of this invention, and the manner of attaining them, will become more apparent and the invention itself will be better understood by reference to the following description of embodiments of the invention taken in conjunction with the accompanying drawings, wherein:

Figure 1 is a schematic diagram of a prior art circuit including a high-side gate driver and a low-side gate driver;

Figure 2 is a schematic diagram of two separate high-side gate drivers and an independent negative substrate potential which supplies the input control logic of the ICs;

Figure 3 is a schematic diagram of two separate high-side gate drivers and a circuit for deriving the independent negative substrate potential ($-V_{cx}$) which supplies the input control logic of the ICs;

Figure 4 is a schematic diagram of two separate high-side gate drivers and another embodiment of a circuit for deriving $-V_{cx}$; and

Figure 5 is a schematic diagram of two separate high-side gate drivers, a circuit for deriving $-V_{cx}$, and a signal translation stage.

Corresponding reference characters indicate corresponding parts throughout the several views. The exemplifications set out herein illustrate embodiments of the invention and such exemplifications are not to be construed as limiting the scope of the invention in any manner.

Referring now to the drawings, Figure 1 illustrates a prior art opposed current power converter 11. The PWM signals are input into the low-side driver circuit 6 after passing through low-side input signal translator transistor 40 and into the high-side circuit 8 driver after passing through high-side input signal translator transistor 42. The input signals communicate with high-side switch 7 and low-side switch 9 to produce on and off conditions. The input signal for high-side switch 7 is received by Schmitt trigger 10 which provides robustness to the logic to make it less sensitive to noisy input signals. NOR gate 18 receives output signals from Schmitt trigger 10 and undervoltage device 20. Undervoltage device 20 functions as an interlock by defeating the drive signal if too little voltage is present. Pulse generator 26 turns on or off in response to a high or low output from NOR gate 18. Pulse generator 26 provides an alternating pulse signal first to translating field effect transistor 27 and then to translating field effect transistor 25. The outputs from translating field effect transistors 25, 27 are sent to receiving stage 30 to set and then reset the corresponding input pins on the flip-flop of receiving stage 30. Undervoltage device 28 is connected to the reset pin on receiving stage 30, and functions as an interlock by defeating the drive signal if too little voltage is present. The output from receiving stage 30 is routed to high-side gate driver 32. High-side gate driver 32 is powered by voltage V_b and voltage V_s. The driving and inverted output from high-side gate driver 32 typically produces one-half (½) to about three (3) amperes of drive. The drive output is fed through resistor R_{gp} to drive high-side switch 7.

The input signal for low-side switch 9 is similarly received by Schmitt trigger 12 connected to time delay block 22. Gate 24 receives output signals from time delay block 22 and undervoltage device 20. Low-side gate driver 34 receives the output from gate 24. Low-side gate driver 34 is powered by voltage V_{cc} 15 and is connected to the common signal of the IC. The driving and inverted output from low-side gate driver 34 drives low-side switch 9 through resistor R_{gn}.

Figure 2 is a schematic diagram of an opposed current power converter driven by two separate high-side driver circuits 8, 8' in accordance with the present invention. The input signal for high-side switch 7 is received by Schmitt trigger 10. NOR gate 18 receives output signals from Schmitt trigger 10 and undervoltage device 20. Undervoltage device 20 functions as an interlock as described above. Pulse generator 26 receives a high or low output from NOR gate 18 indicating when to turn on or turn off. Pulse generator 26 provides an alternating pulse signal first to translating field effect transistor 27 and then to translating field effect transistor 25. The outputs of transistors 25, 27 are sent to receiving stage 30 to set and then reset the corresponding input pins of the flip-flop of receiving stage 30. Undervoltage device 28 is connected to the reset pin on receiving stage 30, and functions as an interlock as described above. The output from receiving stage 30 is routed to high-side gate driver 32, which is powered by voltage V_b and voltage V_s. The driving and inverted output from high-side gate driver 32 typically produces one-half (½) to about three (3) amperes of drive. The drive output of driver 32 is fed through resistor R_g to drive high-side switch 7.

The input signal to high-side driver circuit 8' for low-side switch 9 is translated through the identical logic as the input signal for high-side switch 7. The drive output for low-side switch 9, however, is fed through resistor R_g to drive low-side switch 9.

Battery 48 produces voltage $-V_{cx}$ 13 which supplies the input control logic reference voltage. The logic of the two high-side driver circuits 8, 8' is powered by a simple shunt regulator with Zener diode 46, bypass capacitor 44, and resistor 52 connected to earth ground. It should be understood that the value of the voltage $-V_{cx}$ 13 produced by battery 48 needs to be as negative as the greatest excursion, i.e., most negative value, of the forward voltage across diode D_p 14. Also, it should be known that the common portion is a recitation of the voltage through the diode 14.

Figure 3 illustrates the use of two separate high-side driver circuits 8, 8' similar to that of Figure 2 and represents another embodiment of a circuit for producing $-V_{cx}$ 13. Diode D_p 14 is connected to diode D_1. When a large forward voltage appears across diode D_p 14 at the turn-off of high-side switch 7, diode D_1 begins to conduct because the voltage on the negative side of diode D_1, i.e., the side connected to diode D_p 14, is more negative than $-V_{co}$ 15. Once diode D_1 begins to conduct, $-V_{cx}$ 13 is pulled down the value of V_s during the transient excursion of switch 7. During this excursion, $-V_{cx}$ 13 has a value

which is V_s plus the turn-on voltage of diode D_1. The result is that the voltage levels of -V_{cx} 13 and V_s are very close to each other, and both voltages are more negative than -V_{cc} 15. Diode D_2 provides -V_{cx} 13 during quiescent conditions when the converter is not switching, thereby preventing problems to the IC when not in operation.

Figure 4 illustrates the use of two separate high-side driver circuits 8, 8' as in Figure 2 with an arbitrary AC voltage source 54 to produce -V_{cx} 13. Source 54 is connected to capacitor C_{pump}, which in turn is connected to both diode D_1' and diode D_2. Source 54 could be generated by a separate AC generator or one of several small AC power supplies present in a typical application circuit such as a switched-mode power converter for audio applications. The dotted lines in Figure 4 show two possible points of connection for source 54. Source 54 should operate at the same frequency at which the entire circuit is operating, or some harmonic thereof, to avoid undesirable beat frequencies.

In operation, a current is produced through diode D_2 during the positive voltage swing of source 54. Correspondingly, on the negative voltage swing of source 54, diode D_1' begins to conduct, thereby pulling -V_{cx} 13 down to V_s during the instantaneous excursion of the high-side switch.

Figure 5 includes a signal translation stage 70 for processing the input signals to the gate drivers. Signal translation stage 70 could also have been used with the circuits of Figures 1 through 4. Signal translation stage 70 comprises several, typically three or more, common base stages 71 cascoded together (i.e., the collector of one transistor of a stage 71 is connected to the emitter of the transistor of the next stage 71). Each PWM switch enable signal travels through the emitter of each of its respective common base stages 71 and out the collector. In a practical embodiment, each stage 71 is a divider which is designed to translate the PWM signals down from earth ground before they are input into high-side driver circuits 8, 8'. Several small stages 71 are used to translate the large voltage on the input signals, since small transistors can only translate a portion of the large voltage. On the other hand, small transistors are beneficial because they have low output capacitance.

Each stage 71 includes capacitors 60, 62 for noise reduction. For each additional stage not shown, more capacitors would be present to perform the same function. The base node of each transistor of the chain of stages 71 is bypassed to earth ground, except

for translating transistors Q_{bn} and Q_{bp} which are tied to V_{cc} 15 through resistors 64, 66, respectively. The AC noise incident from the PWM signals exists across the base-collector junctions of translating transistors Q_{bn} and Q_{bp}. Translating transistors Q_{bn} and Q_{bp} carry the current from the PWM signals, and are selected for minimum output capacitance. This permits a minimum disturbance to the collector current when noise is imposed between $-V_{cx}$ 13 and earth ground. Parasitic transistors Q_{cn} and Q_{cp} are used to cancel the noise present in the collectors of translating transistors Q_{bn} and Q_{bp}.

In operation, signal translation stage 70 of Figure 5 produces a current that augments the current flow down through the chain such that a minimum voltage is induced across resistors R_{ip} and R_{in} due to a change in current. An inversion occurs in the voltage across resistors R_{ip} and R_{in} because they are in series with the signal path. In other words, if $-V_{cx}$ 13 instantaneously goes more negative, the voltages across resistors R_{ip} and R_{in} go positive with respect to the input pins of buffers 56, 58, respectively. The voltages across resistors R_{ip} and R_{in} are literally out of phase with $-V_{cx}$ 13. The net noise current seen by R_{ip} and R_{in} pollutes the signals which are incident on buffers 56 and 58. Buffers 56 and 58 are referenced to $-V_{cx}$ 13. This embodiment permits buffers 56 and 58 to cancel out the noise present at their inputs.

The noise voltage across translating transistors Q_{bn} and Q_{bp} is the same voltage that is desired to exist across the transistors Q_{cn} and Q_{cp}. Charging currents are fed back to the chain to cancel the noise in the base-collector capacitance of translating transistors Q_{bn} and Q_{bp}. Translating transistors Q_{bn} and Q_{bp}, however, do not have the same operating point as parasitic transistors Q_{cn} and Q_{cp} because parasitic transistors Q_{cn} and Q_{cp} have no current flow through them. The output capacitance of a transistor is slightly increased when current is flowing through it. Since current is flowing through translating transistors Q_{bn} and Q_{bp}, but not through parasitic transistors Q_{cn} and Q_{cp}, the output capacitances of the transistors are different. This is compensated by connecting the collectors of parasitic transistors Q_{cn} and Q_{cp} to $-V_{cc}$ 15 because that forces the output capacitance of parasitic transistors Q_{cn} and Q_{cp} to increase and compensates for their lack of carrying bias. With this compensation, parasitic transistors Q_{cn} and Q_{cp} form the appropriate nonlinear capacitance to track voltage in the array, and to properly cancel the effects of noise from the $-V_{cx}$ 13 supply line.

While this invention has been described as having a preferred design, the present invention can be further modified within the spirit and scope of this disclosure. This application is therefore intended to cover any variations, uses, or adaptations of the invention using its general principles. Further, this application is intended to cover such departures from the present disclosure as come within known or customary practice in the art to which this invention pertains.

CLAIMS:

1. A gate driver circuit for a half-bridge derived switching power converter having a positive switch (7) coupled to a negative potential (12), and a negative switch (9) coupled to the negative potential (12), the gate driver circuit comprising a first driver circuit (8) for operating the positive switch (7), a second driver circuit (8') for operating the negative switch (9), the gate driver circuit being characterized in that the first and the second driver circuits (8 and 8') have a power input which are referenced to a common potential (13).

2. The gate driver circuit set forth in claim 1 further characterized by a positive potential ($+V_{cc}$) wherein the positive potential and the negative potential define a potential range, the common potential transitioning outside the potential range during operation of the circuit.

3. The gate driver circuit set forth in any previous claim, characterized in that during operation of the circuit, the common potential becomes negative relative to the negative potential.

4. The gate driver circuit set forth in any previous claim, characterized in that the first switch includes a diode (14) connecting the first switch and the negative potential.

5. The gate driver circuit set forth in any previous claim, characterized in that the common potential is a rectification of the voltage through the diode.

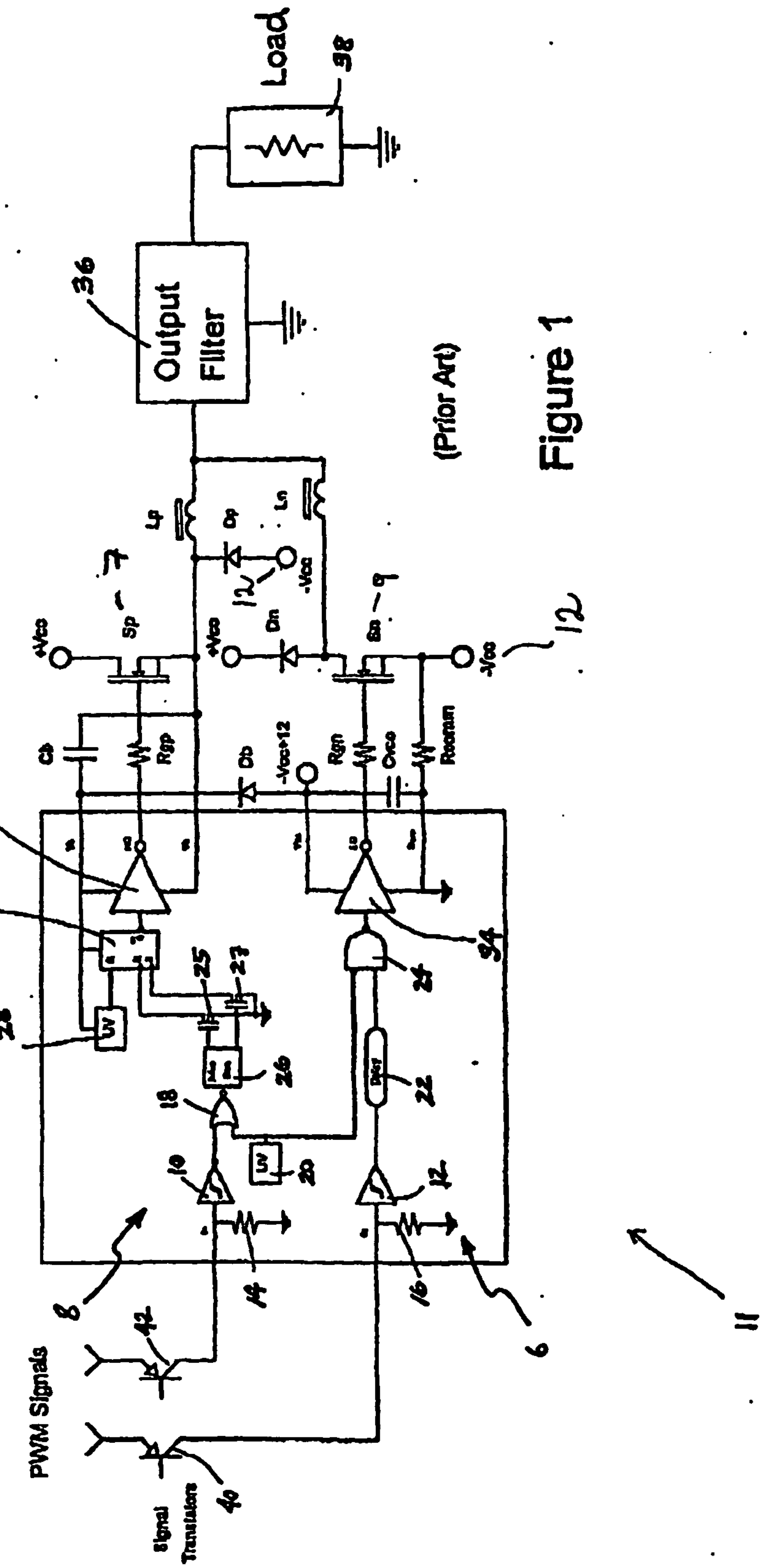
6. The gate driver circuit set forth in any previous claim, characterized in that the common potential is provided by a charge pump (48) referenced to the negative potential and drive by an AC source.

7. The gate driver circuit as set forth in any previous claim, characterized by a signal translation stage (70), the signal translation stage translating a plurality of switch enabling signals from DC potentials, the potentials being positive to the common potential.

8. The gate driver circuit as set forth in claim 7, characterized in that each signal transition stage includes a plurality of three-dimensional semiconductors (71), one of the semiconductors of the signal translation having an input coupled through a capacitance (60, 62) to the power input.

9. The gate driver circuit as set forth in any previous claim, characterized in that the capacitance is the output capacitance of another of the semiconductors of the first signal translation stage.

10. The gate driver circuit as set forth in any previous claim, characterized in that the first driver circuit includes a Schmidt trigger (10), a NOR gate (18), and a pulse generator (26) arranged to generate a signal to a plurality of transistors (25, 27) allowing the first switch to be activated and deactivated in a soft switching manner.



(Prior Art)

Figure 1

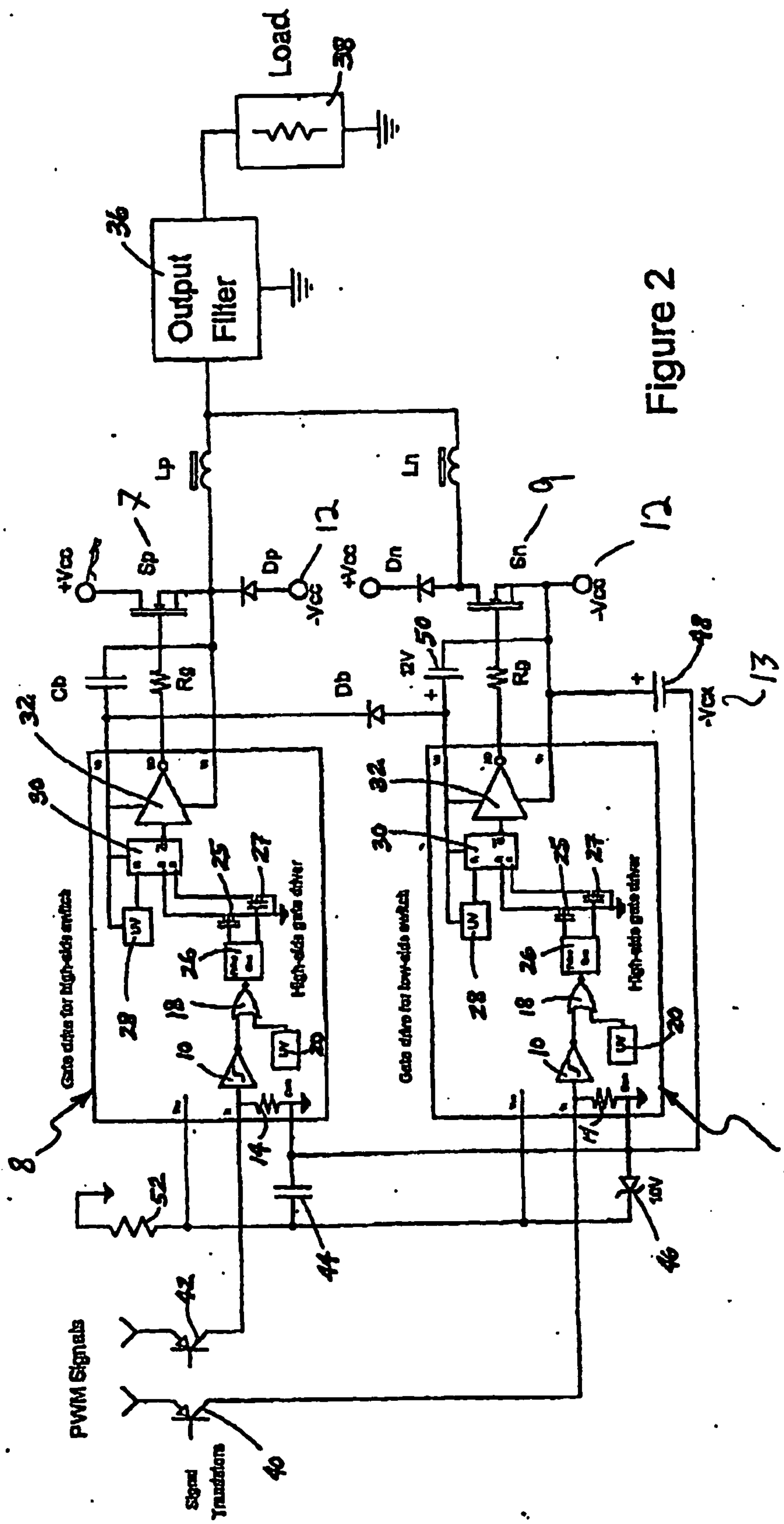

Load
38
Output Filter
36
+Vcc
Sp
7
Lp
Dp
-Vcc
12
+Vcc
Dn
Ln
Sn
9
-Vcc
12
Cb
Rg
Db
12V
50
Rg
48
-Vcc
13
32
30
25
27
26
28
18
10
20
14
Gate drive for high-side switch
High-side gate driver
Gate drive for low-side switch
High-side gate driver
8
8'
52
44
46
10V
42
40
PWM Signals
Signal Translators

Figure 2

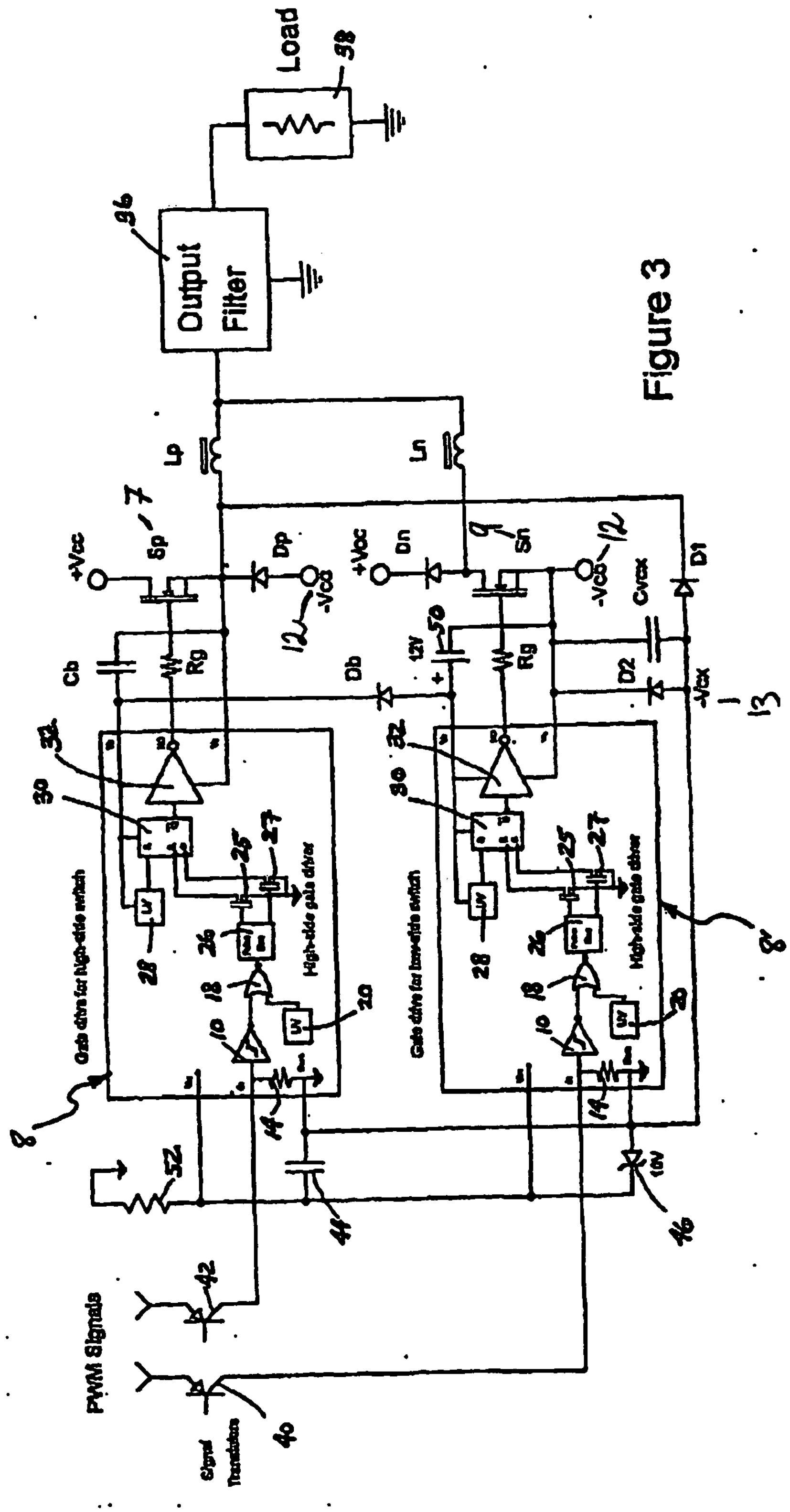


Figure 3

BEST AVAILABLE COPY

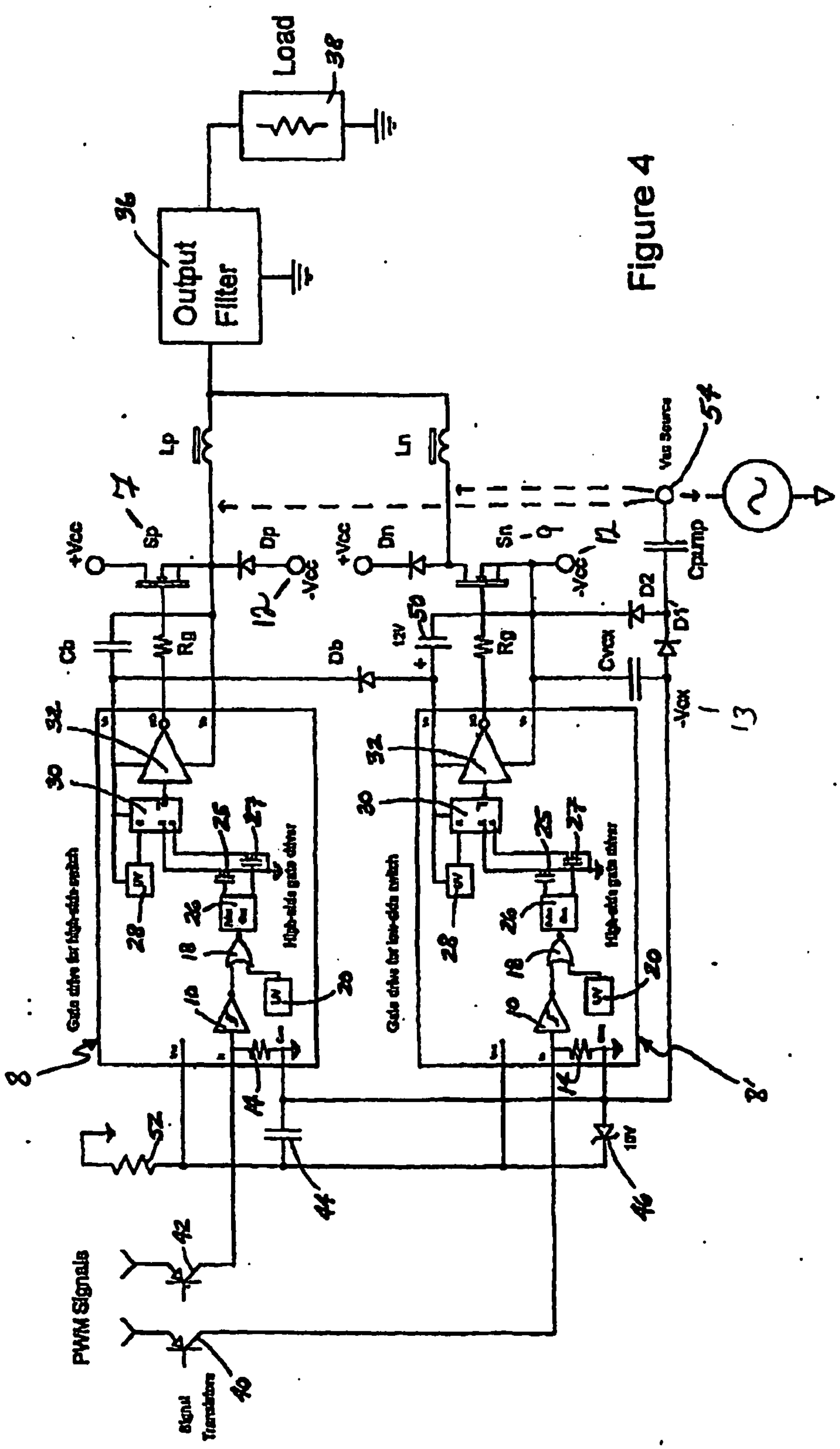

Load
38
36
Output Filter
Lp
Ln
Sp
7
+Vcc
Dp
-Vcc
12
Cb
Rg
32
30
25
27
28
26
18
20
10
Gate drive for high-side switch
High-side gate driver
8
52
14
44
42
PWM Signals
40
Signal Transistors
Dn
Sn
9
Db
12V
50
Cvcx
D2
D1
Cpump
-Vcx
13
Vcx Source
54
Gate drive for low-side switch
46
8'

Figure 4

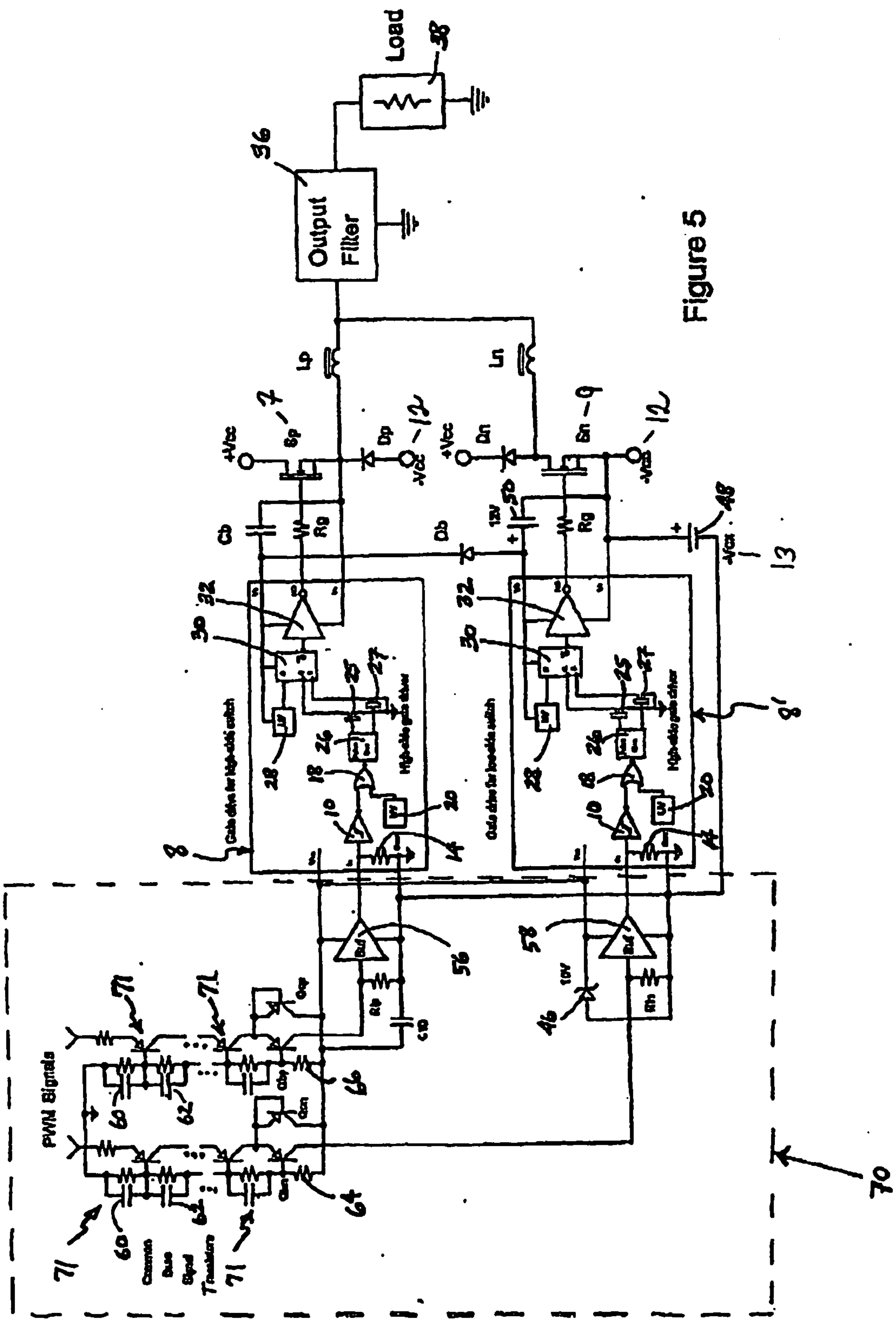


Figure 5

BEST AVAILABLE COPY